APPLICATION NOTE

A linear amplifier (1.6 – 28 MHz) for 8 W PEP in class-A with the BLF175

NCO8705

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CONTENTS

1 SUMMARY
2 INTRODUCTION
3 GENERAL CONSIDERATIONS
4 DESIGN OF THE AMPLIFIER
4.1 Circuit description
4.2 Design procedure
4.2.1 Powergain
4.2.2 Cut-off frequency
4.3 Calculation
4.4 Output matching
4.5 Input matching
5 AMPLIFIER ALIGNMENT
6 AMPLIFIER CONSTRUCTION
6.1 Construction notes
6.2 Heatsink
7 AMPLIFIER PERFORMANCE
7.1 General
7.2 Performance at constant output power
7.3 Performance at constant frequency
8 CONCLUSION
9 REFERENCE
9.1 CIRCUIT DIAGRAM OF THE WIDEBAND LINEAR AMPLIFIER

1 SUMMARY

In this report a description is given of a wideband linear amplifier intended for driver applications in SSB transmitters for the frequency range 1.6 to 28 MHz. It employs a MOS-transistor BLF175 suited for a supply voltage of 50 V.
The transistor is adjusted in class-A with a quiescent drain current of 800 mA. The main properties at P_o = 8 W PEP are:

Powergain: 28.3 – 28.6 dB

IMD (d3): ≤ –41 dB

IMD (d5): ≤ –60 dB

Input return loss: ≤ –26 dB.

2 INTRODUCTION

The amplifier that will be discussed in this report concerns a wideband linear amplifier, designed for driver applications is SSB transmitters in the HF band. This design is based on the RF power MOS-transistor BLF175 which is primarily designed for communication purposes in the HF-band. This device can deliver 8 W PEP in class-A at an IMD (d3) < –40 dB, when operated from a supply voltage of 50 V. It is encapsulated in a SOT123 four-lead flange type with a ceramic cap.

3 GENERAL CONSIDERATIONS

One of the most important factors to be considered in the design of driver stages for SSB transmitters is intermodulation distortion. The major cause for intermodulation distortion is the non-linear transfer characteristic of the transistor.
A generally accepted IM distortion figure is < –40 dB. To achieve this, driver stages must be operated in class-A. One of the properties of a class-A amplifier is its low efficiency, which for pre-drivers is of less importance.

The amplifier must have a flat gain response, within a few tenths of a dB. Its response should preferably be superiour to that of the final amplifier of a SSB transmitter. The input return loss versus frequency must be low because, it will possibly form the load of a pre-driver.

4 DESIGN OF THE AMPLIFIER

4.1 Circuit description

Figure 1 shows the basic circuit of this broadband amplifier. Negative feedback combined with parallel input compensation has been applied to obtain flat gain and low input return loss.

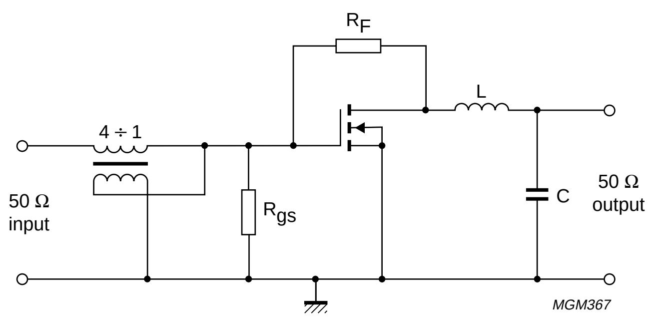


Fig.1 Basic circuit of the wideband amplifier.

Matching of the input to 50 Ω is accomplished with a 4 ÷ 1 broadband transformer of the transmission line type. At the output side a LC-section compensates the output capacitance of the transistor for the frequency range of interest in order to provide the transistor with a constant resistive load.

4.2 Design procedure

The amplifier will be designed for a supply voltage of 50 V and a system impedance of 50 Ω.

First the DC-operating point must be determined. The most important factor that restricts the DC-current in MOS-transistors is the maximum allowable power dissipation in the transistor. For a maximum operating junction temperature of 200 °C and a maximum allowable heatsink temperature of 70 °C the maximum dissipation with R_{thj-h} = 2.9 K/W equals to 44.8 W. This corresponds with a drain current of 0.9 A at V_{ds} = 50 V. In order to keep the dissipation within safe limits I_{ds} is set to 0.8 A.

Second the optimum load resistance is determined. For class-A amplifiers this is given by the relation:

$$R_L = \frac{V_{ds}}{I_{ds}} \qquad (1)$$

In this case R_L equals to $\frac{50}{0.8}$ = 62.5 Ω. In order to avoid an output transformer R_L is chosen to be 50 Ω.

Now the load resistance has been established, the input resistance can be determined. This resistance is formed by the input shunt resistance and that part of the feedback resistance reflected to the input. Several properties of this amplifier are determined by this resistance, viz.:

1. The power gain
2. The cut-off frequency.

In the next sections a brief analysis will be given of this amplifier in order to determine the input resistance and the powergain.

4.2.1 POWERGAIN

For class-A amplifiers small signal analysis produces sufficiently accurate results. The small-signal equivalent circuit of the amplifier is shown in Fig.2. All transistor package parasitics are neglected for this frequency range.

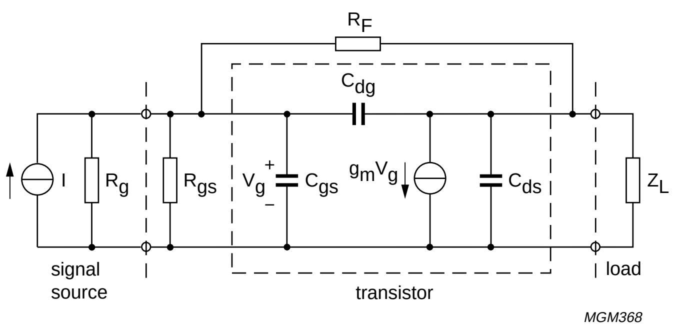


Fig.2 Small signal equivalent circuit of amplifier.

The Y-parameters of the transistor with feedback resistor R_F and shunt resistor R_{gs} are:

$$Y_{11} = G_{gs} + G_F + j\omega(C_{gs} + C_{gd}) \tag{2}$$

$$Y_{12} = -j\omega C_{gd} - G_F \tag{3}$$

$$Y_{21} = g_m - G_F - j\omega C_{gd} \tag{4}$$

$$Y_{22} = G_F + j\omega(C_{ds} + C_{dg}) \tag{5}$$

The general expression for powergain of any linear amplifier is:

$$G_p = \frac{P_o}{P_i} = \frac{G_L|Y_{21}|^2}{|Y_{22} + Y_L|^2 \times \mathrm{Re}(Y_{in})} \tag{6}$$

In which:

$$Y_{in} = Y_{11} - \frac{Y_{12} \times Y_{21}}{Y_{22} + Y_L} \tag{7}$$

The load admittance is:

$$Y_L = G_L - j\omega(C_{ds} + C_{dg}) \tag{8}$$

After substitution of equation (2) to (5) and (7), (8) into (6) we obtain:

$$G_p = \frac{G_L\left[(g_m - G_F)^2 + \omega^2 C_{gd}^2\right]}{(G_L + 2G_F)\left[G_{gs}(G_L + 2G_F) + G_L G + G_F^2 + \omega^2 C_{gd}^2\right]} \tag{9}$$

In which:

$$G = G_F\left(1 + \frac{g_m}{G_L}\right) \tag{10}$$

If G_F and ωC_{gd} are assumed very small with respect to G_L and G_m we get the simple expression:

$$G_p = \frac{g_m^2}{G_L(G_{gs} + G)} \tag{11}$$

4.2.2 CUT-OFF FREQUENCY

The cut-off frequency of this amplifier is dominated by the input circuit. The output circuit has a much higher cut-off frequency and is therefore not relevant. Figure 3 shows the unilaterised small-signal equivalent circuit of Fig.1.

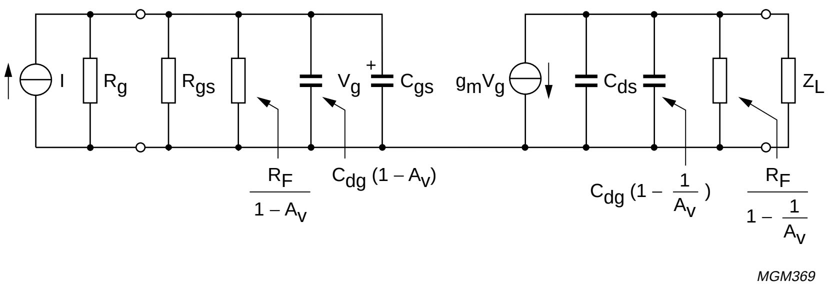


Fig.3 Unilaterised small-signal equivalent circuit.

Av is the voltage gain between drain and gate which is assumed to be a real number. The total input resistance is:

$$R_i = R_{gs} // \frac{R_F}{1 - Av} \tag{12}$$

And the input capacitance is:

$$C_i = C_{gs} + C_{gd}(1 - Av) \tag{13}$$

The 3 dB cut-off frequency of this RC-combination is given by:

$$f_c = \frac{1}{2\pi R_i C_i} \tag{14}$$

So, if C_i is known we can determine R_i for a certain bandwidth.

4.3 Calculation

Calculations are based on transistors from one batch of the BLF175. The mean values of the transistor parameters were taken. These are:

g_m = 1.5 S; (Vds = 10 V; Id = 1 A)

C_{gs} = 145.1 pF

C_{ds} = 34.4 pF; (V_{ds} = 50 V; V_{gs} = 0 V; f = 28 MHz)

C_{gd} = 3.42 pF.

The transconductance (g_m) of this device is determined by a pulse measurement. Under normal operating conditions g_m will be lower due to the higher junction temperature. The reduction is approximately 25% for normal operating conditions. The effective transconductance is therefore:

$g_{me} = 1.5 \times 0.75 = 1.1$ S

The capacitors C_{ds} and C_{gs} are voltage-dependent. Due to RF-excitation the effective capacitance in class-A will be 10% higher, so:

$Cds_e = 1.1 \times C_{ds} = 37.8$ pF
$Cgd_e = 1.1 \times C_{gd} = 3.76$ pF

The voltage gain between drain and gate in Fig.1 can be calculated with:

$$A_V = -g_{me} \times R_L \tag{15}$$

For a load resistance of 50 Ω this amounts to:

$A_v = -1.1 \times 50 = -55$

According to eq. (13) the total input capacitance amounts to:

$C_i = 145.1 + 3.76 \times (1 + 55) = 355.7$ pF

The total input resistance can now be determined with eq. (14). For f = 28 MHz this amounts to:

$$R_i \leq \frac{1}{2 \times \pi \times 28 \times 10^6 \times 355.7 \times 10^{-12}} = 16\ \Omega$$

For the ease of transformation a value of 12.5 Ω has been chosen. The cut-off frequency therefore increased to 35.8 MHz.

R_i consists of the parallel connection of R_{gs} and $R_F/(1–A_v)$ see Fig.3. First the feedback resistance R_F will be calculated. The only restriction that holds for the feedback resistance is the power dissipation in it. This must be kept low in order to prevent deterioration in IMD performance. The dissipation allowed, is set to ≈3% of the RMS output power. According to Fig.3 the total reflected feedback resistance to the output side is:

$$R_F' = \frac{R_F}{1 - \frac{1}{A_v}} \tag{16}$$

Because A_v >>1, $R'_F \approx R_F$ and amounts to:

$R_F = 1500\ \Omega$

Now, R_{gs} can be calculated for $R_i = 12.5\ \Omega$. With $R_F/(1 - A_v) = 26.8\ \Omega$ we find for R_{gs} a value of 23.4 Ω. The closest practical value is 24 Ω.

The powergain in dB can be determined with eq. (9), and is calculated to be:

$G_p = 10 \log (636.6) = 28.4$ dB

When the approximate equation is used (11) we get:

$G_p = 10 \log (756.3) = 28.8$ dB

So, a good estimation is obtained when eq. (11) is used.

4.4 Output matching

The output impedance of the transistor can be represented by a parallel connection of a resistance and a capacitance. The resistance has a value of 50 Ω, see Section *"Design procedure"*, and the capacitance is equal to $1.1 \times (C_{ds} + C_{dg}) = 41.6$ pF due to R_F-excitation. This output capacitance is compensated by a LC-section for the frequency range of interest in order to obtain a constant resistive load, see Fig.4.

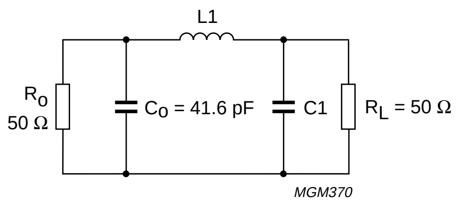


Fig.4 Output matching.

According to Ref. [1] the component values of L_1 and C_1 for a cut-off frequency of 28 MHz are:

$L_1 = 189$ nH and $C_1 = 41.6$ pF with VSWR = 1.05.

The output section contains two additional components, viz.:

1. A drain choke for biasing
2. A dc-blocking capacitor.

For RF-signals the drainchoke is connected in parallel with the output impedance, see Fig.5, and must therefore be large enough, in order to avoid performance degradation at the low end of the band. For the lowest frequency of interest (1.6 MHz) the choke inductance must be at least:

$$L_{ch} = \frac{4R_o}{2\pi f_{min}} \tag{17}$$

In this case L_{ch} amounts to 20 µH. In practice this is obtained by winding 36 turns of enamelled copper-wire (0.7 mm) on a ferroxcube rod, grade 4B1, with a length of 30 mm and a diameter of 5 mm. Because of the open magnetic circuit saturation due to DC-current will hardly occur.

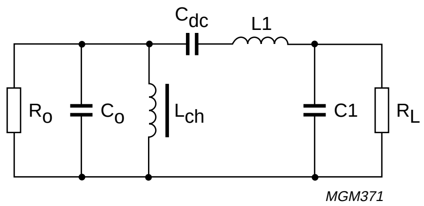


Fig.5 Output section.

The dc-blocking capacitor can be used to compensate the choke inductance for low frequencies. According to [1] this capacitor must be 8 nF for f = 1.6 MHz with $VSWR_{max}$ = 1.03. In practice a chip capacitor was used of 10 nF.

The matching performance of the output section was verified with an impedance analyzer. The transistor was first replaced by a dummy transistor which consisted of a resistor of 50 Ω and a capacitor of 42 pF in a SOT123 header. The return loss was measured at the load connection. It appeared that the return loss improved when C_1 was replaced by a capacitor of 24 pF. This was due to parasitics introduced by the printed circuit board and the additional components like the drainchoke and the blocking capacitor. The return loss was better than –20 dB throughout the band.

4.5 Input matching

The input section is shown in Fig.6.

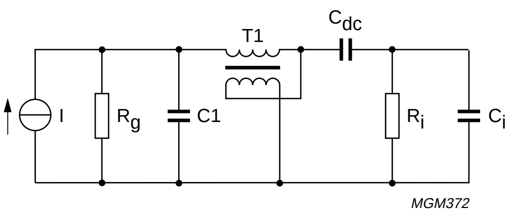


Fig.6 Input section.

A 4 : 1 broadband transformer is applied of the transmission line type. It utilizes a twisted-wire-pair transmission line wound on a toroidal core. The windings are uniformly distributed around the toroid. Figure 7 shows the electrical circuit diagram and constructional details of this transformer.

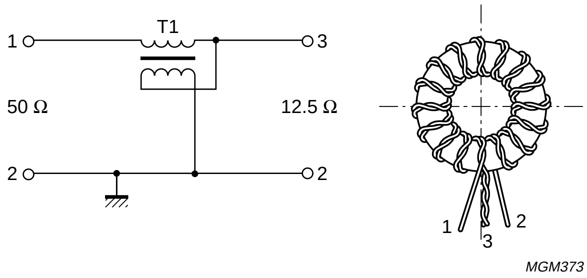


Fig.7 Input transformer.

The required characteristic impedance of the transmission line is:

$$Z_0 = \sqrt{R_g \times R_i}$$

For this case Z_o equals to $\sqrt{50 \times 12.5} = 25\ \Omega$. In practice Z_o will deviate from the required value and compensation will be necessary to improve the broadband performance of the transistor. The characteristic impedance of 25 Ω has been obtained by twisting two enamelled copper wires of 0.25 mm-bare diameter. The wire diameter with isolation included was 0.27 mm. Approximately 10 twists per cm were applied and the total wire length was 25 cm.

A ferroxcube toroid, grade 4C6, has been applied with dimensions (9 × 6 × 3) mm. Here the size is not primarily determined by the power handling capabilities, but the required number of turns needed to establish the parallel inductance between the transformer terminals. On the other hand this inductance must not be higher than necessary, because the broadband performance of the transformer will degrade if the transmission line becomes longer than λ/8. A good practical value is that given by equation (17). This means for the inductance at the 50 Ω side a value of 20 µH and for the 12.5 Ω side a value of 5 µH. The number of turns needed is that which is required to make 5 µH. According to the design information in ref. [2], 13 turns for this toroid were required to make 5 µH. From measurements it appeared to be too low. Therefore the number of turns had to be increased to 18. This is due to deviation in material properties which for smaller toroids is larger.

The dc-blocking capacitor compensates the parallel inductance of 5 µH. For 1.6 MHz, 31.8 nF is necessary according to ref. [1]. Three chip capacitors in parallel were used of 10 nF each.

High frequency compensation for deviation in Z_o is accomplished by parallel capacitors between the transformer terminals. At the low ohmic side a part of C_i provides the required capacitance while at the high ohmic side C_1 provides this. Its value is determined by tuning a variable capacitor for optimum return loss at f = 28 MHz under nominal operating conditions. The required value was 3.9 pF.

5 AMPLIFIER ALIGNMENT

The amplifier was constructed according to the design procedure given in the previous chapter. Measurements were performed throughout the band at an output power of 8 W PEP The results are given below.

Powergain = 27.5 – 28.6 dB

IMD(d3) ≤ –41 dB

IMD(d5) ≤ –60 dB

Input return loss ≤ –18.5 dB.

The highest powergain occurred at f = 1.6 MHz. The total variation in gain of 1.1 dB was found to be relatively large. In order to improve this compensation measures were considered. There were two possibilities, viz.:

1. Parallel input compensation; an inductance in series with the input shunt resistance which increases the effective shunt resistance at high frequencies and hence the gain
2. Feedback compensation: an inductance in series with the feedback resistance witch decreases the feedback at high frequencies and hence improves the gain.

The drawback of the latter is the relatively large inductance required for compensation, a few µH. The former is more elegant because of the low value of the required inductance. Calculation of the optimum inductance for maximally flat response is complicated. Therefore its value was determined in an empirical way. An inductance of 86 nH was found, which reduced the total variation to 0.3 dB for an average gain of 28.4 dB. An additional advantage of this compensation measure was the improvement of the input return loss, which became better than –26 dB.

6 AMPLIFIER CONSTRUCTION

6.1 Construction notes

The circuit diagram and component list are given in Fig.8 and Table 1. The circuit board of this amplifier design is made of two-sided copper clad epoxy fibreglass laminate with a thickness of 1/16 inch and a dielectric constant of 4.5. A full sized pattern of the printed circuit board is shown in Fig.9. The other side is fully metallized and used as ground plane. The ground planes on each side of the board are connected together by means of copper straps at the source leads and the N-connectors and the mounting screws. Figure 9 shows the component layout.
The unavoidable strip in the feedback path represents an inductance of 12 nH and a capacitance of 5.5 pF which can be neglected with respect to the feedback resistance. C4 is a dc-blocking capacitor and should have a low reactance for all frequencies. To prevent low frequency spurious oscillation, a network comprising C7 and R3 is applied. At low frequencies R3 serves as a series loss for choke L2 and thus avoids a high Q factor. C3 and C6 are small bypass capacitors for the carrier frequency. L3 needs to be as large as possible and still be able to handle the required current. C8 must provide a solid bypass at all frequencies including the very low ones.

6.2 Heatsink

The circuit board is attached to a solid brass plate, which is provided with a circular hole for cooling purposes. A water cooling system controls the heatsink temperature.

7 AMPLIFIER PERFORMANCE

7.1 General

Performance measurements were carried out under the following conditions:

Supply voltage: V_{dd} = 50 V

Quiescent drain current: I_{dq} = 0.8 A

Heatsink temperature: T_{hs} = 25 °C

The measuring frequency extends from 1.6 to 32 MHz. Two tones of equal amplitude were used with a frequency separation of 1 KHz. The distortion products were measured with respect to one of the two tones.

7.2 Performance at constant output power

The measurements were done at an output power of 8 W PEP. The results obtained are:

Powergain = 28.3 – 28.6 dB, see Fig.10

IMD (d3) = –41.4 – –47.4 dB, see Fig.11

IMD (d5) = ≤–60 dB

Input return loss ≤–26 dB, see Fig.12.

7.3 Performance at constant frequency

As shown in Fig.11 the worst third order IMD products occurs at the highest end of the band. Therefore, measurements versus output power were only carried out at f = 28 MHz. The results obtained are:

Powergain = 28.1 – 28.4 dB, see Fig.13;

IMD (d3) = –60 – –33.9 dB, see Fig.14 –40 dB is exceeded for $P_o \geq 9.5$ W PEP;

IMD (d5) ≤ –58 dB;

Input return loss ≤ –21.5 dB.

8 CONCLUSION

The design and construction of a wideband linear amplifier has been presented, with the MOS-transistor BLF175, for the frequency range 1.6 – 28 MHz. The transistor is adjusted in class-A and shows good linearity, IMD (d3) ≤ –40 dB, up to an output power of 9.5 W. It is suited for driver applications in SSB transmitters.

9 REFERENCE

[1] H.Nielinger; *“Optimale dimensionering von Breitbandanpassungsnetwerken”*; NTZ 1968, Heft 2, pp. 88–91.
[2] Philips Data handbook; *“Soft Ferrites”*; Book MA01, 1996.

9.1 Circuit diagram of the wideband linear amplifier

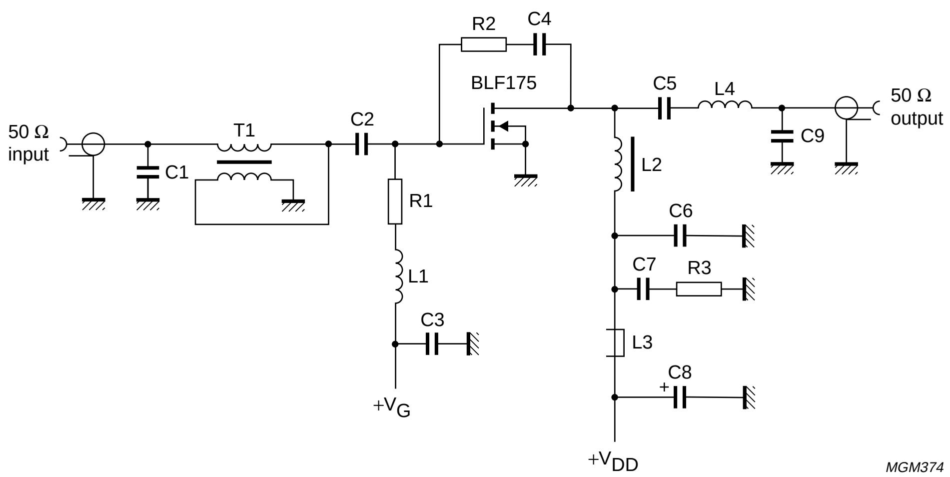


Fig.8 Circuit diagram of the wideband linear amplifier.

Table 1 List of components

Capacitors	
C1 = 3.9 pF	multilayer ceramic chip capacitor; note 1
C2 = 3 × 10 nF	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47103)
C3 = C4 = C6 = 100 nF	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47104)
C5 = 10 nF	multilayer ceramic chip capacitor; (cat.nr. 2222 852 47103)
C7 = 3 × 100 nF	multilayer ceramic chip capacitor; (cat.nr. 2222 852 47104)
C8 = 10 µF (63 V)	Aluminium electrolytic capacitor; (cat.nr. 2222 030 28109)
C9 = 24 pF	multilayer ceramic chip capacitor; note 1
Inductors	
L1 = 86 nH	4 turns enamelled Cu-wire (0.6 mm); int. dia. = 5.0 mm, length = 3.3 mm; leads 2 × 2.0 mm
L2 = 20 µH	drain choke, 36 turns enamelled Cu-wire (0.7 mm) wound on a Ferroxcube rod grade 4B1, dimensions (5 × 30) mm
L3 =	Ferroxcube RF choke, grade 3B (cat.nr. 4312 020 36640)
L4 = 189 nH	8 turns enamelled Cu-wire (1.0 mm); int.dia. = 5.0 mm, length = 9.5 mm; leads 2 × 3.0 mm
Resistor	
R1 = 24 Ω	metal film resistor; 0.4 W
R2 = 1500 Ω	metal film resistor; 0.4 W
R3 = 10 Ω	metal film resistor; 0.4 W
Transformer	
T1 – 4 : 1 transformer	18 turns of twisted pair of 0.25 mm enamelled Cu-wire (10 twists per cm) wound on a toroidal core grade 4C6, dimensions (9 × 6 × 3) mm. (cat.nr. 4322-020-97171)
Printed circuit board: double sided Cu-clad epoxy fibreglass laminate (ε_r = 4.5), thickness 1/16 inch	

Note

1. American technical ceramics capacitor type 100B.

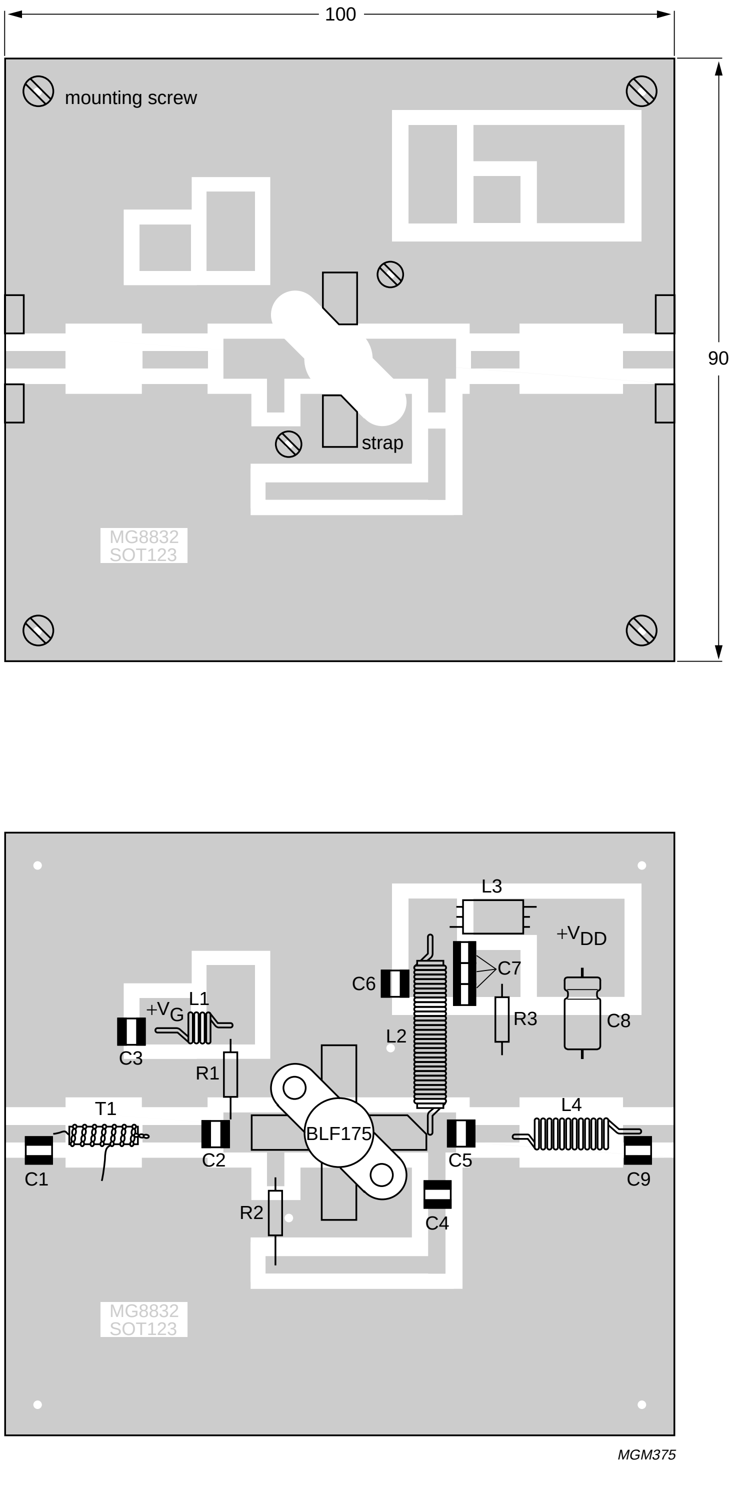
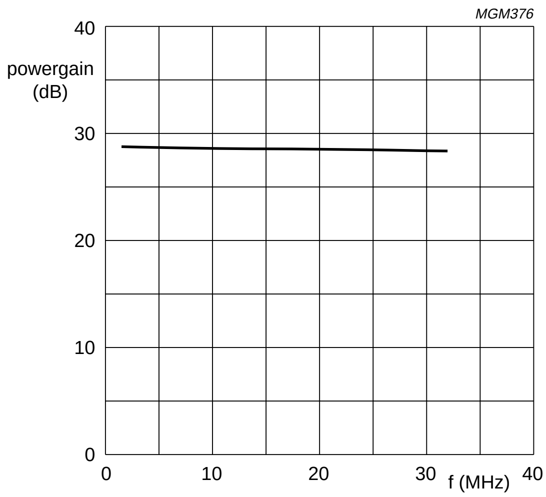


Fig.9 Printed circuit board and component layout.



Conditions:
V_{ds} = 50 V
I_{dq} = 800 mA
P_o = 8 W PEP
T_h = 25 °C.

Fig.10 Powergain versus frequency.

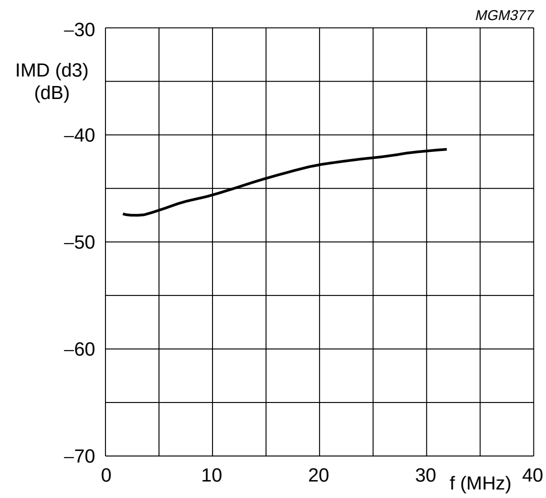
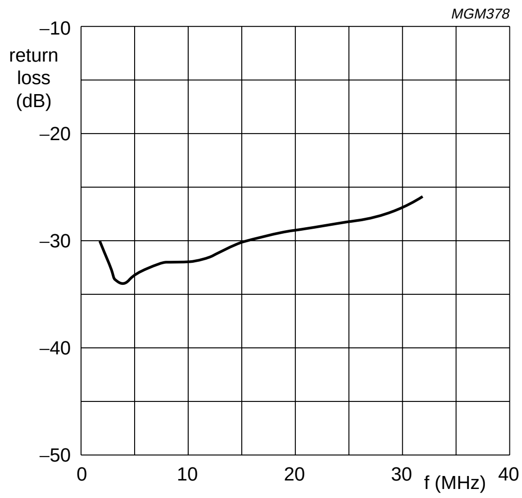


Fig.11 3rd order IMD versus frequency.



Conditions: V_{ds} = 50 V, I_{dq} = 800 mA, Po = 8 W PEP, Th = 25 °C
Tone separation = 1 kHz.

Fig.12 Input return loss versus frequency.

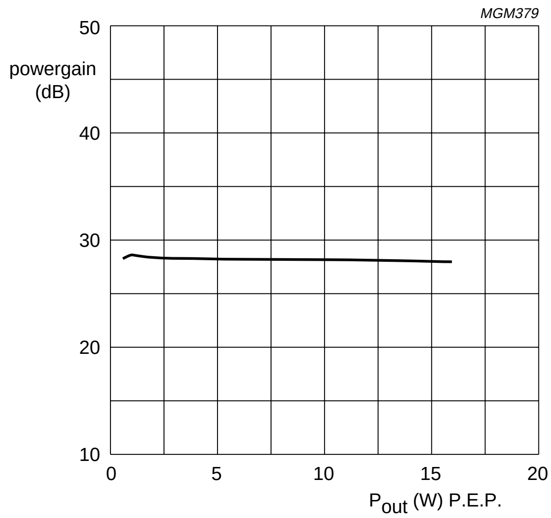
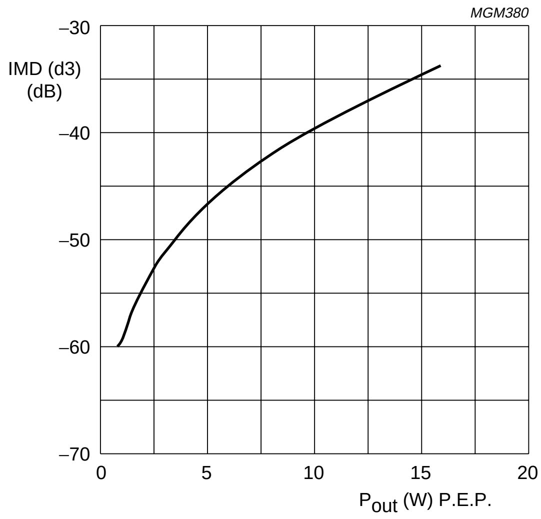


Fig.13 Powergain versus output power.



Conditions: V_{ds} = 50 V, I_{dq} = 800 mA, Th = 25 °C, f = 28 MHz (p–q = 1 kHz).

Fig.14 3th order IMD versus output power.

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